



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/724,384

11/26/2003

Mark M. Leather

00100.01.0025

9662

29153 7590 06/03/2008
ADVANCED MICRO DEVICES, INC.
C/O VEDDER PRICE P.C.
222 N.LASALLE STREET
CHICAGO, IL 60601

EXAMINER

LAY, MICHELLE K

ART UNIT

PAPER NUMBER

2628

MAIL DATE

DELIVERY MODE

06/03/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/724,384	Applicant(s) LEATHER ET AL.	
	Examiner MICHELLE K. LAY	Art Unit 2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4,6-9,12,14-17,20 and 22-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4,6-9,12,14-17,20 and 22-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

The amendment filed 03/31/2008 has been entered and made of record. Claims 1, 4, 6-9, 12, 14-17, and 20-26 are pending.

Response to Arguments

Applicant's arguments, filed 03/31/2008, have been fully considered and are persuasive. The non-final rejection filed 11/29/2007 has been withdrawn.

Information Disclosure Statement

The information disclosure statement(s) (IDS) submitted on 03/31/2008 is being considered by the examiner.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims **17**, **20**, and **22-24** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Although the claim language is acceptable, Applicant describes in the disclosure in [0108; 0062, 0063] (newly amended specification filed 03/31/2008) that the computer program product can be a carrier wave. Thus, in light of the specification, claims 17, 20, and 22-24 recite[s] a signal *per se*. Claims that recite nothing but the physical characteristics of a form of energy, such

as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism, *per se*, and as such are nonstatutory natural phenomena. O'Reilly, 56 U.S. (15 How.) at 112-14. Moreover, it does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in §101.

As a suggestion to overcome this 101 rejection, the disclosure can be amended to not associate the computer program product with carrier waves and to only limit the computer program product to the examples mentioned in paragraph [00108] of Applicant's disclosure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1, 4, 7-9, 12, 14-17, 20, and 22-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosman et al. (6,222,550 B1) in view of Blythe et al. (2002/0145612 A1), Storm et al. (5,999,196), and Sperber et al. (6,557,083).

Rosman teaches the limitation of claims 1, 4, 7-9, 12, 14-17, 20, and 22-26 with the exception explicitly teaching a unified shader, single graphics chip and defining tiles of the output screen. However, Sperber teaches an integrated-circuit die in which a processor core and graphics core are integrated on a single chip and Blythe teaches

dividing the frames into subareas that are allocated to different rendering pipelines.

Additionally, Storm teaches a unified shader.

In regards to claims **1**, **9**, **17** and **25**, Rosman teaches a 3D graphics processor having parallel pipelines. A hardware accelerated Geometry Engine (said **front-end**) may supply the vertices of triangles to triangle setup engine (28) [c.6 L.25-32]. The triangle setup engine (28) [Fig. 3] directs the gradients and vertices to the triangle pixel-pipelines (40,41) (said **directing said geometry into pipelines**) [c.6 L.33-35]. Once a triangle is setup by triangle setup engine (28), its gradients and vertices are sent to the next available triangle pixel-pipeline(s) (40,41) (said **back-end**). Triangle pixel-pipelines (40,41) are each pixel engines (PE) that receive the three vertices for a triangle. Triangle pixel pipelines (40,41) output pixel values to a frame buffer [c.6 L.33-45].

Blythe teaches a geometry distributor (102; Fig. 1) that divides the compositing window (said **output screen**) into subareas (said **tile**) and conveys the defining parameters to each of the PGUs (108) (said **pipelines**) [0071]. Additionally, PGU assignor (204) assigns one or more PGU (108) to each of the subareas [0072]. It would have been obvious to one of ordinary skill in the art to tile the output screen of Rosman because the spatial compositing increases the rate at which an overall frame is rendered [Blythe: 0046].

Storm teaches a method of processing 3D graphics commands comprising, as shown in Fig. 2, a graphics accelerator (112) receiving stream of input vertex packets from the host 102 [c.5 L.3-21], and performing shading operations on the vertexes. As

shown in Fig. 3, Storm teaches the shading operations comprising ALU/memory pair (floating point blocks 152s, and SRAM 153s) to perform both texture operations and color operations from the received vertex packets (which include texture and color information, c.5,L.17-21) [c.12 L.28-67], and writing received texture values to the memory SRAM 153 [c.5 L.45-54] (said ***unified shader***). It would have been obvious to one of ordinary skill in the art to utilize the method of implementing ALU/memory pair to perform both texture and color operations as taught by Storm in combination with the method of shading as taught by Rosman in order to reduce the bottleneck in 3D graphics processing [Storm: c.1 L.49-61], and thereby improving overall graphics accelerator performance.

Sperber teaches an integrated-circuit die in which a processor core (310) and graphics core (320) are integrated on a single chip [Fig. 3; c.4 L.20-35].

Therefore, it would have been obvious to one of ordinary skill is the art to implement the modified Geometry Engine of Rosman in view of Blythe and Storm into the processor core of Sperber, and the pixel-pipelines of Rosman into the graphics core of Sperber because it is known in the art that significant amount of rendering causes a burden on the bandwidth of the memory channel, which in turn can reduce the performance of the graphics system. Furthermore, memory demands by the graphic engine can reduce CPU performance, as well as other units [Sperber: c.2 L.13-31]. Thus, by implementing both the front-end and back-end of Rosman on a single chip, the interfaces between units are reduced in size, resulting in a faster interaction.

Art Unit: 2628

Additionally, the single chip occupies less real estate within the system, therefore providing either a smaller system overall, or more space for other internal devices.

In regards to claims **4**, **12**, and **20**, Rosman teaches FIFO (32) buffers [c.6 L.55-60].

In regards to **6**, **14**, and **22**, Rosman teaches z-buffering [c.6, L.65-68]. Additionally, the method/system of Rosman generates pixel colors and writes the colors into a buffer (said **color buffer**) [c.4 L.1-13].

In regards to claims **7**, **8**, **15**, **16**, **23**, and **24**, the 3D graphics processor of Rosman generates vertex color, texture and other attributes as well as other gradients. Rosman further teaches utilizing multiple rendering pipes. It would have been obvious to one of ordinary skill in the art that the implicit z-buffer as utilized by Rosman needed to perform depth functions would function with the shader and the scan converter in order to generate a single 3-D display. Furthermore, the “early” and “late” z-interface is within the same z-buffer, Thus the “early” and “late” z-interface is dependent and defined on the step process that the generation occurs.

In regards to claim **26**, Rosman teaches a raster engine (34) (said, **rasterizer**), span engine (30) (said **scan converter**), register (42) stores triangle attributes (said **texture unit**), registers (42,44) [c.6 L.46-64]. Furthermore, one or more triangle setup engine(s)

receives triangle primitives from a host or geometry engine and generates vertex color, texture and other attributes as well as their gradients [*abstract*].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle K. Lay whose telephone number is (571) 272-7661. The examiner can normally be reached on Monday-Friday 7:30a-5p.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee M. Tung can be reached on (571) 272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michelle K Lay/
Examiner, Art Unit 2628
05/30/2008 /mkl/

/Kee M Tung/
Supervisory Patent Examiner, Art
Unit 2628